Amendments to the Claims

The listing of the claims will replace all prior version, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An oscillator circuit, which comprises:

a tank circuit having a first port and a second port, the tank circuit configured to resonate at one or more predefined frequencies;

a first oscillator transistor having a first port, a second port coupled to the first port of the tank circuit, and a third port;

a second oscillator transistor having a first port, a second port coupled to the second port of the tank circuit, and a third port; ~~and~~

a gain-cell tuning inductor coupled between the third ports of the first and second oscillator transistors;

a first capacitor coupled between the third port of the first oscillator transistor and the second port of the tank circuit; and

a second capacitor coupled between the third port of the second oscillator transistor and the first port of the tank circuit,

wherein the gain-cell tuning inductor is operable to conduct a bias signal supplied thereto to the third ports of the first and second oscillator transistors.

Claim 2 (original): The oscillator circuit of claim 1, further comprising a supply resistor having a first port coupled to the first ports of the first and second oscillator transistors.

Claim 3 (canceled).

Claim 4 (original): The oscillator circuit of claim 1, wherein the tank circuit comprises:

first and second varactor diodes coupled in series and between the first and second ports of the tank circuit; and

a tank inductor coupled between the first and second ports of the tank circuit.

Claim 5 (original): The oscillator circuit of claim 1, wherein the tank inductor is coupled to first potential, and the first ports of first and second oscillator transistors are coupled to a second potential.

Claim 6 (original): The oscillator circuit of claim 5, wherein the first and second oscillator transistors comprise PMOS FET transistors or p-type bipolar transistors.

Claim 7 (original): The oscillator circuit of claim 6, wherein the first potential is ground potential and the second potential ranges from +2.7 to +3.6 VDC.

Claim 8 (original): The oscillator circuit of claim 5, wherein the first and second oscillator transistors comprise NMOS FET transistors or n-type bipolar transistors.

Claim 9 (original): The oscillator circuit of claim 8, wherein the first potential ranges from +2.7 to +3.6 VDC, and the second potential is ground potential.

Claim 10 (currently amended): An integrated oscillator circuit, which comprises:

a tank circuit having a first port and a second port, the tank circuit configured to resonate at one or more predefined frequencies;

a first oscillator transistor having a first port, a second port coupled to the first port of the tank circuit, and a third port;

a second oscillator transistor having a first port, a second port coupled to the second port of the tank circuit, and a third port;

a first capacitor coupled between the third port of the first oscillator transistor and the second port of the tank circuit;

a second capacitor coupled between the third port of the second oscillator transistor and the first port of the tank circuit; and

a bias supply circuit configured to generate a biasing signal, comprising:

a bias transistor having a first port, a second port, and a third port, wherein the second and third ports are coupled together;

a first bias circuit resistor coupled to the first port of the bias transistor;

a second bias circuit resistor coupled to the second port of the bias transistor; and

a gain-cell tuning inductor coupled between the third ports of the first and second oscillator transistors, and coupled to the second port of the bias transistor to receive the biasing signal,

wherein the gain-cell tuning inductor is operable to conduct the bias signal to the third ports of the first and second oscillator transistors.

Claim 11 (original): The integrated oscillator circuit of claim 10, further comprising a supply resistor having a first port coupled to the first ports of the first and second oscillator transistors.

Claim 12 (canceled).

Claim 13 (original): The integrated oscillator circuit of claim 10, wherein the tank circuit comprises:

first and second varactor diodes coupled in series and between the first and second ports of the tank circuit; and

a tank inductor coupled between the first and second ports of the tank circuit.

Claim 14 (original): The oscillator circuit of claim 10, wherein the second bias circuit resistor and the tank inductor are coupled to first potential, and the first bias circuit resistor and the first ports of first and second oscillator transistors are coupled to a second potential.

Claim 15 (original): The oscillator circuit of claim 14, wherein the first and second oscillator transistors comprise PMOS FET transistors or p-type bipolar transistors.

Claim 16 (original): The oscillator circuit of claim 15, wherein the first potential is ground potential and the second potential ranges from +2.7 to +3.6 VDC.

Claim 17 (original): The oscillator circuit of claim 14, wherein the first and second oscillator transistors comprise NMOS FET transistors or n-type bipolar transistors.

Claim 18 (original): The oscillator circuit of claim 17, wherein the first potential ranges from +2.7 to +3.6 VDC, and the second potential is ground potential.

Claim 19 (currently amended): An oscillator circuit comprising:

tank circuit means for resonating at one or more predefined frequencies, the tank circuit means having a first port and a second port;

gain cell means for providing negative impedance to compensate losses in the tank circuit; the gain cell means comprising:

a first oscillator transistor having a first port, a second port coupled to the first port of the tank circuit, and a third port;

a second oscillator transistor having a first port, a second port coupled to the second port of the tank circuit, and a third port; and

gain-cell tuning means for increasing the open-loop gain of the gain cell means, the gain cell tuning means coupled between the third ports of the first and second oscillator transistors,

a first capacitor coupled between the third port of the first oscillator transistor and the second port of the tank circuit; and

a second capacitor coupled between the third port of the second oscillator transistor and the first port of the tank circuit,

wherein the gain-cell tuning means is operable to conduct the bias signal to the third ports of the first and second oscillator transistors.

Claim 20 (canceled).